

What is claimed is:

1. A semiconductor device comprising:
 - a substrate having an insulating layer formed thereon;
 - a silicon layer having a thickness t_s formed on the insulating layer, the silicon layer including a first area having a first impurity concentration of $D_f \text{ cm}^{-3}$, and a second area having a second condition of $D_p \text{ cm}^{-3}$;
 - a fully-depleted MOSFET formed in the first area of the silicon substrate; and
 - a partially-depleted MOSFET formed in the second area of the silicon layer;

wherein the semiconductor device satisfies the following condition:

$$28 \text{ nm} \leq t_s \leq 42 \text{ nm}$$

$$D_f \leq 9.29 * 10^{15} * (62.46 - t_s)$$

$$D_f \leq 2.64 * 10^{15} * (128.35 - t_s)$$

$$D_p \geq 9.29 * 10^{15} * (62.46 - t_s)$$

$$D_p \geq 2.64 * 10^{15} * (129.78 - t_s).$$

2. A semiconductor device according to claim 1, wherein the device satisfies condition of $D_f \leq 3.00 * 10^{15} * (102.67 - t_s)$.

3. A semiconductor device according to claim 1, wherein the device satisfies condition of $D_p \geq 3.29 * 10^{15} * (125.70 - t_s)$.

4. A semiconductor device according to claim 1, wherein the thickness of the silicon layer has a range 38 nm to 42 nm, the impurity concentration D_f is equal or more than $1.9 * 10^{17} \text{ cm}^{-3}$, and the impurity concentration D_p is equal or less than $2.2 * 10^{17} \text{ cm}^{-3}$.

5. A semiconductor device according to claim 1, wherein the thickness of the silicon layer has a range 33 nm to 37 nm, the impurity concentration of D_f is equal or less than $2.5 * 10^{17} \text{ cm}^{-3}$, and the impurity concentration D_p is equal or more than $2.7 * 10^{17} \text{ cm}^{-3}$.

6. A semiconductor device according to claim 1, wherein the thickness of the silicon layer has a range 28 nm to 32 nm, the impurity concentration of D_f is equal or less than $2.7 * 10^{17} \text{ cm}^{-3}$, and the impurity concentration D_p is equal or more than $3.2 * 10^{17} \text{ cm}^{-3}$.